REMARKS

As a preliminary matter, Applicants appreciate the Examiner's allowance of claims 23-25.

Claims 6-14 and 18-22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamazaki (U.S. Patent No. 5,576,729). In response, Applicants amended independent claim 6 to clarify that the storing of the polarity patterns occurs in a read only memory (ROM), and amended claim 10 to define the polarity pattern storing portion as having a ROM. Applicants traverse the rejection as it applies to independent claim 18 because Yamazaki fails to disclose (or suggest) changing a polarity pattern, which detects a polarity of a data signal supplied to data bus lines, from a first polarity pattern to a second polarity pattern when a rate of flicker patterns exceeds a predetermined value.

The Examiner asserts that Yamazaki teaches in FIG. 1, item 36 a polarity pattern storing portion that stores polarity patterns. The memory element 36 of Yamazaki is formed of a RAM. (See col. 9, ln. 53). Yamazaki fails to disclose (or suggest) a polarity pattern storing portion having a ROM, or a step of storing polarity patterns in a ROM of a polarity pattern storing portion. For these reasons, withdrawal of the § 102(b) rejection of independent claims 6 and 10 and their respective dependent claims 7-9 and 11-13 is respectfully requested.

In independent claim 18 of the present Application, as shown is the seventh embodiment of the present invention, for example, there is a drive mode detecting portion 102a. The drive mode detecting portion 102a checks a state (i.e., a pattern) of turned-ON

picture elements and turned-OFF picture elements of two pixels (i.e., 6 picture elements) which are adjacent in the horizontal direction, and it is decided whether the state is a "flicker pattern" or not. For example, as described in Applicants' Specification on page 80, lines 3-11, when the G picture element in one pixel of the two pixels being aligned in the horizontal direction is turned ON and the G picture element in the other pixel is not turned ON, such a pattern is decided as a flicker pattern. Further, the number of flicker patterns contained in a predetermined region of the display screen (or, the rate of flicker patterns) is calculated, and it is decided whether the number of the flicker patterns (i.e., the number of the specific state of turned-ON picture elements and turned-OFF picture elements) exceeds a predetermined number or not.

On the other hand, Yamazaki shows in FIG. 1 and discloses in claim 3 and at col. 12, lines 6-17 that the circuits 34, 38, 40, 42 and the memory element 36 are used to calculate the number of pixels whose on/off-status changes when the scanning electrode is changed from Y_n to Y_{n+1}. In Yamazaki, it is decided whether the number of pixels whose on/off-status has changed exceeds a predetermined number or not.

Thus, the operation performed in calculating a rate of flicker patterns contained in at least one block, and when the rate exceeds a predetermined value, as recited in claim 18 of the present Application, is not disclosed or suggested by Yamazaki. For this reason, withdrawal of the § 102(b) rejection of claims 18-22 is respectfully requested.

For all of the foregoing reasons, Applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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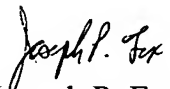
By 
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